REMARKS

Applicants respectfully request further examination and reconsideration in view of the above amendments. Please cancel Claim 13 without prejudice. Claims 1-3, 5-9, 12 and 18-20 remain pending in the case. Claims 1-3, 5-9, 12 and 18-20 are rejected. Claims 1, 3, 5-9, 12 and 18-20 are amended herein. No new matter has been added.

35 U.S.C. §103(a)

The instant Office Action states that Claims 1-3, 5-9, 12 and 18-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over United States Patent 5,437,017 by Moore et al., hereinafter referred to as the "Moore" reference, in view of "IBM Technical Disclosure Bulletin, May 1994, Vol. 37, Issue 5, pages 249-250, hereinafter referred to as the "IBM" reference. Applicants have reviewed the cited references and respectfully submit that the embodiments of the present invention as recited in Claims 1-3, 5-9, 12 and 18-20 are patentable over Moore in view of IBM for the following rationale.

Applicants respectfully submit that Moore does not show or suggest an indication that a target instruction has been translated into a host instruction, as recited in the claims. More specifically, the claimed indication is associated with a memory address for a target instruction that has been translated into a host instruction, but nevertheless the claimed indication is an indication that a target instruction has been so translated. The claimed indication maintains coherency

between a target instruction and a host instruction translated from that target instruction, in essence by preventing the target instruction from being overwritten before the host instruction is updated, invalidated or removed, as recited in the claims.

As understood by the Applicants, Moore only maintains coherency between a virtual address and a physical address translated from the virtual address. At best, Moore's translation lookaside buffer invalidate (TLBI) instruction appears to suggest an indication that an entry within the translation lookaside buffer (TLB) is invalid. That is, at best, Moore can perhaps be read as providing an indication whether the translation between a virtual address and a physical address is valid or invalid. However, the claimed indication is not concerned with the translation between a virtual address and a physical address. As noted above, the claimed indication pertains to the translation between a target instruction and a host instruction.

In contrast to the present claimed invention, Moore does not show or suggest a host instruction that is translated from a target instruction; indeed, this fact is admitted to on page 3 of the instant Office Action. If Moore does not show or suggest translations of target instructions to host instructions, then by no means can Moore show or suggest an indication associated with such translations.

The IBM reference is cited to teach a target instruction that has been translated into a host instruction. First, Applicants respectfully submit that the IBM reference does not teach that which it is relied upon as teaching, as discussed further below. Second, Applicants respectfully submit that, even if for the sake of argument one could conclude that Moore or IBM or the combination thereof teaches the translation of target instructions into host instructions, neither Moore nor IBM nor the combination thereof shows or suggests an indication associated with a translation of a target instruction to a host instruction. To reiterate, Applicants respectfully submit that Moore and IBM (alone or in combination) do not show or suggest the claimed indication, which as claimed is associated with a translation between a target instruction and a host instruction.

As mentioned above, Applicants respectfully submit that the IBM reference does not teach that which it is relied upon as teaching. The IBM reference appears to describe a SYNC instruction that is broadcast from a sending processor to a number of receiving processors. Applicants respectfully submit that the act of broadcasting an instruction does not equate to translating an instruction. Furthermore, Applicants respectfully submit that the IBM reference makes no mention of the receiving processors translating the SYNC instruction. Indeed, the receiving processors are only required to acknowledge receipt of the SYNC instruction – the SYNC instruction is not even executed by the receiving processors. Therefore, Applicants respectfully submit that, for the

purpose of teaching translating target instructions to host instructions, the IBM reference adds nothing to the Moore reference.

In summary, Applicants respectfully submit that Moore and IBM, alone or in combination, do not show or suggest "means for providing an indication whether a first memory address to be written stores a target instruction which has been translated to at least one host instruction that is stored at a second memory address," "means for providing an indication whether a target memory address to be written stores a target instruction which has been translated to a host instruction that is stored at a host memory address," "marking a memory address for a target instruction which has been translated to a host instruction," or "means for indicating whether a physical address stores an instruction of a target instruction set which has been translated to an instruction of a host instruction set" as recited in independent Claims 1, 7, 12 and 18, respectively.

Therefore, Applicants respectfully submit that the basis for rejecting Claims 1, 7, 12 and 18 under 35 U.S.C. § 103(a) is traversed and that Claims 1, 7, 12 and 18 are in condition for allowance. Because Claims 2-3, 5-6, 8-9, and 19-20 depend from either Claim 1, 7, 12 or 18, Applicants respectfully submit that the basis for rejecting Claims 2-3, 5-6, 8-9 and 19-20 under 35 U.S.C. § 103(a) is also traversed, as these claims are dependent on an allowable base claim.

Conclusions

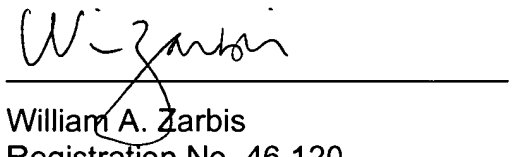
In light of the above remarks, Applicants respectfully request reconsideration of the rejected claims.

Based on the arguments presented above, Applicants respectfully assert that Claims 1-3, 5-9, 12 and 18-20 overcome the rejections of record and, therefore, Applicants respectfully solicit allowance of these claims.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,
WAGNER, MURABITO & HAO L.L.P.

Dated: 6/9, 2006



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